Sub D1

Q2

5. (Amended) A stacked semiconductor storage device as claimed in claim 2, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

6. (Amended) A stacked semiconductor storage device as claimed in claim 4, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

7. (Amended) A stacked semiconductor storage device as claimed in claim 1, wherein said wiring substrate is a sheet wiring substrate.

8. (Amended) A stacked semiconductor storage device as claimed in claim 1, wherein said wiring substrate is a board wiring substrate.

REMARKS

The specification has been amended to address the informality noted by the Examiner. Additionally, the specification and abstract have been amended to conform with U.S. practice, employ more idiomatic English and correct minor clerical errors. No new matter has been entered by any of the foregoing amendments.

The claims have been amended to address the 112 rejection, and also to clarify that the semiconductor storage device is a stacked semiconductor storage device, and that the wiring substrate has wiring patterns thereon. Support is found, for example, in Figs. 2-4 of the original application. It is submitted that the claims have not been limited within the meaning of Festo.

Turning to the art rejections, all of the claims have been rejected as being anticipated by Takiar et al or as anticipated by Warren. It is submitted that neither Takiar et al nor Warren teaches a stacked semiconductor storage device in which a wiring substrate having wiring patterns thereon is interposed between the lower chip and the upper chip, for relaying electric

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connection between the upper chip and the substrate as required by claim 1. In fact, the only suggestion of a wiring pattern is found in Fig. 2 of Takiar et al. However, in Takiar et al, the wiring pattern (strip contact 68) is formed on the top chip. And, Takiar et al runs long leads from the top chip to the leads 44, 64 of the carrier member. Thus, Takiar et al is similar to the Fig. 1 prior art in Applicant's specification.

Warren is no better. Warren teaches relaying electrical connections between an upper multichip decal 14 superimposed on an underlying integrated circuit 12, which in turn is stacked on a substrate 11. Electrical connections between the upper decal 14 and the substrate 11 are made using a three-bond, daisy-chained wedge bond 20 on bonding pads 13 carried on the lower integrated circuit 12. In Applicant's claimed invention, electric connection is relayed between the upper chip and the substrate through the wiring patterns of the wiring substrate interposed between the upper chip and the lower chip. Thus, neither Takiar et al nor Warren can be said to anticipate, or for that matter, suggest the claimed invention.

Pursuant to 37 CFR 1.121, marked copies of the amended specification pages, abstract and amended claims showing the change made therein accompany this amendment.

Having dealt with all of the objections raised by the Examiner, the application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,

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MARKED COPY OF SPECIFICATION PAGES
1-7

SERIAL NO. 09/593,891

DOCKET: NEC DP-624

SEMICONDUCTOR STORAGE DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor storage device. More [to] particularly, this invention relates to wiring structure of the semiconductor storage device according to stack type MCP (Multi Chip Package) of superimposing a plurality of chips.

Description of the Prior Art

Formerly, [the]a stack MCP [to be]package is formed in such a way that a plurality of chips are superimposed. Namely, [the]a stack MCP consists of the package [of causing]in which a plurality of chips [to be] are superimposed. In [the]a stack MCP, generally, a bonding pad of respective chips is arranged in a place near by, with the same arrangement. Further, it is necessary that respective chip sizes are [the] of optimum size. In recent years, it is required a combination of memory with various capacities.

In order to [reply]meet this requirement, for instance, [the]Japanese Patent Application Laid-Open No. HEI 5-121643 discloses a bonding method. Such [the]bonding method is that bonding is performed at the position where bonding pad position of the chip side is shifted largely.

Fig. 1 is a view showing a conventional stack MCP.

In Fig. 1, a package substrate 1, a lower chip 2, and an upper chip 3 are placed one upon another while being shifted from the lowest layer. A bonding pad 4 of the upper chip 3 is connected to a bonding pad 5 of the package substrate 1 by a bonding wire 6. A bonding pad 7 of the lower chip 2 is connected to a bonding pad 5 of the package substrate 3 by a bonding wire 8.

As described above, in [the]a conventional stack MCP, the bonding wire 6 from the upper chip 3 is connected directly to the package substrate 1 exceeding the lower chip 2,

therefore, extremely long bonding wire [3]6 is necessary. For that reason, the bonding wire [3]6 deviates from prescribed position on the occasion of confining [to be enclosed] the bonding wire [according to the] in resin, thus there is the problem of [existing danger of the] breaking [down of]a wire or of contact [of]with another wire [therebetween].

Further, there is the problem that thickness of the package is forced to be increased because the bonding wire increases in the height direction for the sake of wire bonding of long distance.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present invention, in order to overcome the above-mentioned problem to provide a semiconductor storage device which enables various plural memories to be mounted on the same package, further in the case where even though scale of respective chips and / or position of the bonding pad are different, it is capable of providing [the] a stack MCP in which the chips are superimposed.

According to a first aspect of the present invention, in order to achieve the above-mentioned object, there is provided a semiconductor storage device constituted in such a way that [it causes] a lower chip and an upper chip are superimposed on a substrate, which comprises a wiring substrate for relaying electric connection between the upper chip and the substrate which wiring substrate is provided between the lower chip and the upper chip.

According to a second aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein there are provided a first terminal connected to a terminal on a surface of the upper chip, a second terminal connected to a terminal on a surface of the substrate, and a wiring pattern for connecting the first and the second terminals on the surface of the wiring substrate.

According to a third aspect of the present invention, in the second aspect, there is provided a semiconductor storage device, which further comprises a first bonding wire for connecting the terminal of the surface of the upper chip with the first terminal, and a second bonding wire for connecting the terminal of the surface of the substrate with the second terminal.

According to a fourth aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein there is provided a wiring pattern whose one end is connected to a terminal on a rear surface of the upper chip, and whose other terminal is connected to a terminal on a surface of the lower chip.

According to a fifth aspect of the present invention, in the second or the fourth aspect, there is provided a semiconductor storage device, wherein the terminal of the surface of the lower chip is connected to the terminal of the surface of the substrate by a third bonding wire.

According to a sixth aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein the wiring substrate is a sheet [shape] wiring substrate.

According to a seventh aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein the wiring substrate is a board [shape] wiring substrate.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with accompanying drawings. It should be expressly understood, however, that the drawings are for purpose of illustration only and are not intended as a definition of the limit of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a [constitution] perspective view showing a conventional stack MCP;

Fig. 2 is a [constitution] perspective view showing a first embodiment of the present invention;

Fig. 3 is a [constitution] prespective view showing a second embodiment of the present invention; and

Fig. 4 is an enlarged fragmentary view of a single bonding pad of Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described in detail in accordance with the accompanying drawings.

Fig. 2 shows [constitution of the] construction of a stack MCP (Multi Chip Package) according to the first embodiment of the present invention. The present embodiment, as illustrated, is characterized in that, in the stack type MCP, a wiring sheet 9 intervenes between an upper chip 3 and lower chip 2, thus the bonding wires 10, 11 are connected from the upper chip 3 to the package substrate 1 [while relaying this] via the wiring sheet 9.

Namely, in Fig. 2, there is provided the wiring sheet 9 between the upper chip 3 and the lower chip 2. There are provided a first bonding pad 12 and a second bonding pad 13 [at] on the wiring sheet 9. Further, there is provided a wiring pattern 14 for connecting these bonding pads 12, 13. Furthermore, the bonding pad 4 of the upper chip 3 is connected to the above-described bonding pad 12 by the first bonding wire 10. Moreover, the second bonding pad [thirteen] 13 is connected to the bonding pad 5 of the package substrate 1 by the bonding wire 11.

According to the above [constitution] construction, the signal from the upper chip 3 is transmitted to the package substrate 1 [while relaying] via the wiring sheet 9. Namely, the

signal from the upper chip 3 is transmitted to the bonding pad 4, the bonding wire 10, the bonding pad 12, the wiring pattern 14, the bonding pad 13, the bonding wire 11, and the bonding pad 5. Oppositely, transmission of the signal from the package substrate 1 to the upper chip is implemented in the opposite order to the order described above.

Consequently, according to the present embodiment, in the case where a differential of chip size is large between the upper chip 3 and the lower chip 2, wire length does not become long, thus it is capable of avoiding the problem concerning the package combination such as wire deviation and so forth described above. Further, in large number of cases, the stack MCP shares the signal both of the upper chip 3 and the lower chip 2, combination between chips whose arrangement of the bonding pads becomes easy by employing the wiring substrate 9. Namely, due to the wiring pattern 14 on the wiring sheet 9, it is [capable of putting] possible to locate the wire of the upper chip 3 [to] adjacent periphery of the bonding pad 7 of the lower chip 2 through which the common signal flows.

Next, there will be described the second embodiment of the present invention. In the above-described [the] first embodiment, the [constitution is that it causes]construction places the rear surface of the upper chip 3 [to be placed] on the surface of the wiring sheet 9. However, in the present embodiment, the upper chip 3 is placed on the wiring sheet 9 in such a way that chip surface is directed to the lower direction while causing inside and outside to be reversed before placing on the wiring sheet 9. Further, one end of the wiring pattern 14 of the wiring sheet 9 is connected directly to the bonding pad 4 of the upper chip 3, while the other end of the wiring pattern 14 is connected to the bonding pad 7 of the lower chip 2.

According to the above-described [constitution] construction, the bonding pad 4 is connected directly to the wiring pattern 14 on the wiring sheet 9. Consequently, [the] a

bonding [falls into disuse with respect to] wire between the wiring sheet 9 [from] and the upper chip 3 becomes unnecessary.

Further, [it causes] by extending the wiring pattern on the wiring sheet 9 to [be lengthened] run to the upper part of the bonding pad 7 of the lower chip 2, [thus forming the pad such that the bonding pad 7 of the lower chip 2 exposes . Thereby,] as shown in Fig. 4, it becomes possible to perform bonding both of the bonding pad 7 of the lower chip 2 and the wiring pattern 14 on the wiring sheet 9 to the bonding pad 5 of the package substrate 3 with one [time of] wire bonding step.

As described above, according to the present embodiment, it becomes possible to [remove] eliminate the wire bonding with respect to the wiring sheet 9 from the upper chip 3, [it is capable of getting thin the] and to obtain a thinner package [further]. As shown in Fig. 3, when the arrangement of the bonding pad 4 of the upper chip 3 is perpendicular to the arrangement of the wiring sheet 9, the lower chip 2, and respective bonding pad of the package substrate 1 in the horizontal direction, since it becomes [to remove the] possible to eliminate wiring bonding [to] in the horizontal direction, [there is obtained the effect of causing] it becomes possible to reduce the size of the [horizontal direction of the] package [to be reduced] in the horizontal direction.

Further, in the above described [the] first and the second embodiments, description is implemented with respect to wiring sheet as the wiring substrate, however, it is also suitable that the wiring substrate is of the board type [one].

As described above, according to the present invention, there is provided [the] a wiring substrate such as the wiring sheet and so forth between the upper chip and the lower chip, thus causing electric connection to the package substrate from the upper chip to be implemented

through the above described wiring substrate, therefore, even though the differential of [the] chip size between the upper chip and the lower chip is large, it becomes possible to [move] position the bonding pad to the ideal bonding position.

For that reason, it is capable of developing easily the stack MCP of chips of combination which it is impossible to assemble until now because the differential of the chip size is large.

Consequently, it is capable of mounting various plural memories on the same package, thus even though when scale of respective chips and / or the position of the bonding pad are different, it is capable of providing the stack MCP in which the chips are superimposed.

Further, in the cases where the upper chip and the lower chip are [performed bonding] bonded to the same bonding pad on the package substrate, even though respective chip layouts are different and the bonding pads on the chip exist in the positions with long distance, it is [capable of arranging] possible to arrange the bonding pad by changing wiring on the wiring sheet to the ideal bonding position.

While preferred embodiments of the invention have been described using specific terms, the description has been for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.

MARKED COPY OF AMENDED CLAIMS

SERIAL NO. 09/593,891

DOCKET: NEC DP-624

MARKED CLAIMS SHOWING CHANGES MADE:

1. (Amended) A stacked semiconductor storage device [constituted in such a way that it causes] comprising, in combination, a lower chip and an upper chip [are] superimposed on a substrate, said semiconductor storage device further comprising:

a wiring substrate having wiring patterns thereon, interposed between said lower chip and said upper chip, for relaying electric connection between said upper chip and said substrate [which wiring substrate is provided between said lower chip and said upper chip].

2. (Amended) A stacked semiconductor storage device as claimed in claim 1, wherein there are provided a first terminal connected to a terminal on a surface of said upper chip, a second terminal connected to a terminal on a surface of said substrate, and a wiring pattern for connecting said first and said second terminals on the surface of said wiring substrate.

3. (Amended) A stacked semiconductor storage device as claimed in claim 2, further comprising:

a first bonding wire for connecting said terminal of the surface of said upper chip with said first terminal; and

a second bonding wire for connecting said terminal of the surface of said substrate with said second terminal.

4. (Amended) A stacked semiconductor storage device as claimed in claim 1, wherein there is provided a wiring pattern whose one end is connected to a terminal on a rear surface of said upper chip, and whose other terminal is connected to a terminal on a surface of said lower chip.

5. (Amended) A stacked semiconductor storage device as claimed in claim 2, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

6. (Amended) A stacked semiconductor storage device as claimed in claim 4, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

7. (Amended) A stacked semiconductor storage device as claimed in claim 1, wherein said wiring substrate is a sheet [shape] wiring substrate.

8. (Amended) A stacked semiconductor storage device as claimed in claim 1, wherein said wiring substrate is a board [shape] wiring substrate.

MARKED COPY OF ABSTRACT

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ABSTRACT

A semiconductor storage device enables various plural memories to be mounted on the same package, and even though size of respective chips and / or position of bonding pad are different, it is capable of providing a stack MCP in which the chips are superimposed. It causes wiring sheet to intervene between an upper chip and a lower chip. There are provided [a] bonding [pad 12, a bonding pad 13] pads and a wiring pattern for connecting these bonding pads in the wiring sheet. A bonding pad [4] of the upper chip is connected to the bonding pad [12] by a first bonding wire, while the bonding pad [13] is connected to a bonding pad [5] of the package substrate by a second bonding wire. According to this [constitution] construction, the signal from the upper chip is transmitted to the package substrate [while relaying by] via the wiring sheet.